

## **LOW-CURRENT AND HIGH-SPEED PHASE-CHANGE MEMORY DEVICES AND METHODS OF DRIVING THE SAME**

### **Abstract of the Disclosure**

Phase-change memories in which phase is changed by varying the resistance  
5 by a small amount are provided. In the phase-change memory, a set state is defined as  
a state where amorphous nuclei are formed in a phase-change layer of a memory cell  
and the phase-change layer has an initial resistance that is higher than in a crystalline  
matrix, and a reset state is defined as a state where the number and/or the density of  
the amorphous nuclei are greater than those in the set state and a resistance is higher  
10 than in the set state. A current for writing the reset and set states is reduced to several  
hundred microamperes, and a period required for writing the reset and set states is  
reduced to several tens of nanoseconds to several hundred nanoseconds.